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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/618,971	GUPTA, VIKRAM	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 31-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 31-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

DETAILED ACTION

1. This communication is in response to the Applicants' Amendment and Response mailed on May 23, 2004. Claims 1, 3, 31, 33, 34, 35, 36 and 38 were amended. Claims 20-30 were deleted. Claims 1-19 and 31-43 of the application are pending. This office action is made final.

Response to Arguments

2. Applicants' amendments filed on May 23, 2004 have been fully considered. In response to claim amendments made, the art rejections based on the additional prior art are included in this office action. Examiner's response to Applicant's arguments is presented in Paragraph 13 below.

Drawings

3. The set of drawings mailed on May 21, 2004 does not include sheet 2 for Figure 3. The Applicant is directed to send corrected sheet 2 to overcome the objections indicated in the previous Office Action.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507).

6.1 **IN** teaches microprocessor based mixed signal field programmable integrated device and prototyping methodology. Specifically as per Claim 1, **IN** teaches a method of designing an integrated circuit having digital and analog circuit portions, the digital and analog circuit portions each having defined functions (CL1, L26-32); comprising:

providing an emulation circuit which has a configuration capable of being modified (CL1, L7-11; CL1, L21-22; CL2, L14-19; CL2, L22-26);

affixing the emulation circuit on a test substrate (CL1, L63 to CL2, L4; CL2, L30-39);

providing a version of the analog circuit portion having at least some of the defined functions of the analog circuit portion (CL1, L63 to CL2, L4);

affixing the analog circuit version on the test substrate (CL1, L63 to CL2, L4);

testing the analog circuit version (CL2, L4-6; CL1, L36-37; CL2, L30-39) while modifying the configuration of the emulation circuit (CL1, L21-22; CL2, L14-19; CL2, L22-26; CL1, L63-66); and

providing the digital circuit portion, the design of which is based on the testing of the analog circuit version (CL1, L35-36; CL2, L30-39; the programmable digital portion allows modifying the design of the digital portion based on the testing of the analog circuit version); while modifying the configuration of the emulation circuit (CL1, L21-22; CL2, L14-19; CL2, L22-26; CL1, L63-66).

IN does not expressly teach providing an emulation circuit, which is capable of generating noise. **BO** teaches providing an emulation circuit, which is capable of generating noise (Abstract; CL1, L19-30; CL1, L58-63), as generating and applying noise permits evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included

providing an emulation circuit, which was capable of generating noise, as generating and applying noise would permit evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit.

As per Claim 2, **IN** teaches modifying the analog portion in response to the testing step (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

6.2 As per Claim 3, **IN** and **BO** teach the method of claim 1. **IN** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion is obtained (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

IN does not expressly teach repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained. **BO** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained (CL1, L50-54), as that would minimize

performance degradation of an analog or mixed signal integrated circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained, as that would minimize performance degradation of an analog or mixed signal integrated circuit.

6.3 As per Claim 4, **IN** and **BO** teach the method of claim 1. **IN** teaches providing a version of the digital circuit portion having all of the defined functions of the digital circuit portion (CL1, L35-36; CL2, L30-39); and

affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion (CL1, L63 to CL2, L4; CL2, L30-39).

IN does not expressly teach affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions. **BO** teaches affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions (CL1, L50-54), as that would minimize performance degradation of an analog or mixed signal

integrated circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions, as that would minimize performance degradation of an analog or mixed signal integrated circuit.

As per Claim 5, **IN** teaches that the digital circuit portion providing step includes testing the defined functions of the digital circuit portion separately from the analog circuit portion (CL1, L32-39; CL2, L30-39).

As per Claim 6, **IN** teaches that the digital circuit portion testing includes programming an FPGA for testing the defined functions of the digital circuit portion (CL1, L41-43; CL1, L63-66).

As per Claim 7, **IN** teaches that the digital circuit portion testing includes simulating the defined functions of the digital circuit portion (CL1, L36; CL2, L30-39).

6.4 As per Claim 19, **IN** and **BO** teach the method of claim 1. **IN** does not expressly teach that the number of gates in the emulation circuit is substantially equivalent to a number of gates in the digital circuit portion. **BO** teaches that the number of gates in the emulation circuit is substantially equivalent to a number of gates in the digital circuit portion (Abstract, L3-5), as that

permits noise to be generated representative of the digital switching noise generated by the digital integrated circuit (Abstract, L3-5). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included the number of gates in the emulation circuit being substantially equivalent to a number of gates in the digital circuit portion, as that would permit noise to be generated representative of the digital switching noise generated by the digital integrated circuit.

6.5 As per Claim 36, **IN** teaches an integrated circuit having digital and analog portions (CL1, L26-32); designed by a process comprising:

providing an emulation circuit which comprises a circuit path that may be modified (CL1, L7-11; CL1, L21-22; CL2, L14-19; CL2, L22-26);

affixing the emulation circuit on a test substrate (CL1, L44; CL2, L30-39);

providing a version of the analog circuit portion having at least some of the defined functions of the analog circuit portion (CL1, L63 to CL2, L4);

affixing the analog circuit version on the test substrate (CL1, L63 to CL2, L4); and

testing the analog circuit version (CL2, L4-6; CL1, L36-37; CL2, L30-39) while modifying the circuit path in the emulation circuit (CL1, L21-22; CL2, L14-19; CL2, L22-26; CL1, L63-66); and

providing the digital circuit portion, the digital portion having a configuration based on the testing of the analog circuit (CL1, L35-36; CL2, L30-39; the programmable digital portion allows modifying the design of the digital portion based on the testing of the analog circuit

version); while modifying the circuit path in the emulation circuit (CL1, L21-22; CL2, L14-19; CL2, L22-26; CL1, L63-66).

IN does not expressly teach providing an emulation circuit, which generates noise. **BO** teaches providing an emulation circuit, which generates noise (Abstract; CL1, L19-30; CL1, L58-63), as generating and applying noise permits evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the design process of **IN** with the design process of **BO** that included providing an emulation circuit, which generates noise, as generating and applying noise would permit evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit.

As per Claim 37, **IN** teaches modifying the analog portion in response to the testing step (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

6.6 As per Claim 38, **IN** and **BO** teach the integrated circuit of claim 37. **IN** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit

portion is obtained (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

IN does not expressly teach repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained. **BO** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained (CL1, L50-54), as that would minimize performance degradation of an analog or mixed signal integrated circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the design process of **IN** with the design process of **BO** that included repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained, as that would minimize performance degradation of an analog or mixed signal integrated circuit.

6.7 As per Claim 39, **IN** and **BO** teach the integrated circuit of claim 36. **IN** teaches providing a version of the digital circuit portion having all of the defined functions of the digital circuit portion (CL1, L35-36; CL2, L30-39); and

affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion (CL1, L63 to CL2, L4; CL2, L30-39).

IN does not expressly teach affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions. **BO** teaches affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions (CL1, L50-54), as that would minimize performance degradation of an analog or mixed signal integrated circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the design process of **IN** with the design process of **BO** that included affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions, as that would minimize performance degradation of an analog or mixed signal integrated circuit.

6.8 As per Claim 43, **IN** and **BO** teach the integrated circuit of claim 36. **IN** does not expressly teach that the number of gates in the emulation circuit is substantially equivalent to a

number of gates in the digital circuit portion. **BO** teaches that the number of gates in the emulation circuit is substantially equivalent to a number of gates in the digital circuit portion (Abstract, L3-5), as that permits noise to be generated representative of the digital switching noise generated by the digital integrated circuit (Abstract, L3-5). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN** with the integrated circuit of **BO** that included the number of gates in the emulation circuit being substantially equivalent to a number of gates in the digital circuit portion, as that would permit noise to be generated representative of the digital switching noise generated by the digital integrated circuit.

7. Claims 8 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), and further in view of **Abiko et al. (AB)** (U.S. Patent 5,193,070).

7.1 As per Claim 8, **IN** and **BO** teach the method of claim 1. **IN** and **BO** do not expressly teach the emulation circuit comprises at least one array comprising at least one shift register. **AB** teaches the emulation circuit comprises at least one array comprising at least one shift register (CL4, L31-38; CL4, L60-67; CL5, 12-14; Cl5, L65 to Cl6, L8; CL6, L8-9), as shift registers permit shifting the contents of the register by specified number of bits (CL6, L8-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** and **BO** with the method of **AB** that included the emulation circuit

comprises at least one array comprising at least one shift register, as that would permit shifting the contents of the register by specified number of bits.

7.2 As per Claim 40, **IN** and **BO** teach the integrated circuit of claim 36. **IN** and **BO** do not expressly teach the emulation circuit has at least one array comprising at least one shift register. **AB** teaches the emulation circuit has at least one array comprising at least one shift register (CL4, L31-38; CL4, L60-67; CL5, 12-14; Cl5, L65 to Cl6, L8; CL6, L8-9), as shift registers permit shifting the contents of the register by specified number of bits (CL6, L8-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN** and **BO** with the integrated circuit of **AB** that included the emulation circuit comprises at least one array comprising at least one shift register, as that would permit shifting the contents of the register by specified number of bits.

8. Claims 9-13, 15 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507) and **Abiko et al. (AB)** (U.S. Patent 5,193,070), and further in view of **Porteners et al. (PO)** (U.S. Patent application 2001/0049806).

8.1 As per Claim 9, **IN, BO** and **AB** teach the method of claim 8. **IN, BO** and **AB** do not expressly teach that the testing the analog circuit version is performed while alternately shutting off and turning on at least one array. **PO** teaches that the testing the analog circuit version is performed while alternately shutting off and turning on at least one array (Page 1, Para 2, Para 3,

Para 7, Para 8), as that allows the macros to be tested individually for design and test efficiency (Page 1, Para 2, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the testing the analog circuit version is performed while alternately shutting off and turning on at least one array, as that would allow the macros to be tested individually for design and test efficiency.

8.2 As per Claim 10, **IN, BO** and **AB** teach the method of claim 8. **IN, BO** and **AB** do not expressly teach that the shift register comprises a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit. **PO** teaches that the shift register comprises a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4), as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit allow scan chains and seam circuits to be built for circuit testing (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the shift register comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit, as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit would allow scan chains and seam circuits to be built for circuit testing.

IN, BO and **AB** do not expressly teach that the shift register comprises a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern. **PO** teaches that the shift register comprises a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4), as such plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern allow scan chains and seam circuits to be built for mixed signal testing in circuits involving analog and digital macros (Page 1, Para 5; Page 2, Para 14, Para 23). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the shift register comprising a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern, as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit, as such plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern would allow scan chains and seam circuits to be built for mixed signal testing in circuits involving analog and digital macros.

8.3 As per Claim 11, **IN, BO, AB** and **PO** teach the method of claim 10. **IN, BO** and **AB** do not expressly teach that the testing the analog circuit version is performed while applying a signal at the clock input. **PO** teaches that the testing the analog circuit version is performed while applying a signal at the clock input (Page 2, Para 14, Para 23; Page 3, Para 25), as that allows the analog and digital circuits to be divided into independent subfunction macros and tested individually using independent clock signals for analog and digital circuits (Page 1, Para 2 and 3; Page 3, Para 25). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the testing the analog circuit version being performed while applying a signal at the clock input, as that would allow the analog and digital circuits to be divided into independent subfunction macros and tested individually using independent clock signals for analog and digital circuits.

8.4 As per Claim 12, **IN, BO, AB** and **PO** teach the method of claim 11. **IN, BO** and **AB** do not expressly teach that the testing the analog circuit version is performed while varying the clock input signal. **PO** teaches that the testing the analog circuit version is performed while varying the clock input signal (Page 2, Para 14, Para 23; Page 3, Para 25), as that allows the data bits to be moved along the flip flops serially from the first clock domain to the second clock domain under the control of the first and second clock signals for testing analog and digital macros (Page 2, Para 14 and 23). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the testing the analog circuit version being performed while varying the clock

input signal, as that would allow the data bits to be moved along the flip flops serially from the first clock domain to the second clock domain under the control of the first and second clock signals for testing analog and digital macros.

Per Claim 13: **IN** teaches the testing the analog circuit version is performed while varying the data pattern (CL3, L41-44).

8.5 As per Claim 15, **IN, BO, AB** and **PO** teach the method of claim 10. **IN, BO** and **AB** do not expressly teach that the interconnecting blocks comprise a plurality of logic paths, wherein each logic path is comprised of differing amounts of logic gates, and wherein the testing of the analog circuit portion is performed while alternately selecting from among the plurality of logic paths. **PO** teaches that the interconnecting blocks comprise a plurality of logic paths, wherein each logic path is comprised of differing amounts of logic gates, and wherein the testing of the analog circuit portion is performed while alternately selecting from among the plurality of logic paths (Page 1, Para 2, Para 3, Para 7; Page 2, Para 23; Page 3, Para 24 and Para 25), as that allows the analog and digital circuits to be divided into independent subfunction macros and tested individually (Page 1, Para 2 and 3). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the interconnecting blocks comprising a plurality of logic paths, wherein each logic path was comprised of differing amounts of logic gates, and wherein the testing of the analog circuit portion was performed while alternately selecting from among the

plurality of logic paths, as that would allow the analog and digital circuits to be divided into independent subfunction macros and tested individually.

8.6 As per Claim 41, **IN, BO** and **AB** teach the integrated circuit of claim 40. **IN, BO** and **AB** do not expressly teach that the shift register comprises a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit. **PO** teaches that the shift register comprises a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4), as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit allow scan chains and seam circuits to be built for circuit testing (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO** and **AB** with the integrated circuit of **PO** that included the shift register comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit, as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit would allow scan chains and seam circuits to be built for circuit testing.

IN, BO and **AB** do not expressly teach that the shift register comprises a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern. **PO** teaches that the shift register comprises a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting

logic blocks sequentially, and wherein the data bits form a data pattern (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4), as such plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern allow scan chains and seam circuits to be built for mixed signal testing in circuits involving analog and digital macros (Page 1, Para 5; Page 2, Para 14, Para 23). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO** and **AB** with the integrated circuit of **PO** that included the shift register comprising a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern, as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit, as such plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern would allow scan chains and seam circuits to be built for mixed signal testing in circuits involving analog and digital macros.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), **Abiko et al. (AB)** (U.S. Patent 5,193,070), and **Porteners et al. (PO)** (U.S. Patent application 2001/0049806) and further in view of **Ungar (UN)** (U.S. Patent 5,563,524).

9.1 As per Claim 14, **IN, BO, AB** and **PO** teach the method of claim 10. **IN, BO, AB** and **PO** do not expressly teach that the interconnecting logic blocks comprise Exclusive-Or gates, and wherein the testing the analog circuit version is performed while varying the data pattern using the Exclusive-Or gates. **UN** teaches that the interconnecting logic blocks comprise Exclusive-Or gates, and wherein the testing the analog circuit version is performed while varying the data pattern using the Exclusive-Or gates (CL4, L21-32), as that allows the shift register to be configured for different modes of operation and pseudo random signal generation (CL4, L31-32; L22). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO, AB** and **PO** with the method of **UN** that included the interconnecting logic blocks comprising Exclusive-Or gates, and wherein the testing the analog circuit version was performed while varying the data pattern using the Exclusive-Or gates, as that would allow the shift register to be configured for different modes of operation and pseudo random signal generation.

10. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), **Abiko et al. (AB)** (U.S. Patent 5,193,070), and **Porteners et al. (PO)** (U.S. Patent application 2001/0049806) and further in view of **Lee (LE)** (U.S. Patent RE37,500).

10.1 As per Claim 16, **IN, BO, AB** and **PO** teach the method of claim 10. **IN, BO, AB** and **PO** do not expressly teach that at least one of the flip-flops is coupled to an equal number of

pads through an equal number of output drivers, which may be enabled and disabled. **LE** teaches that at least one of the flip-flops is coupled to an equal number of pads through an equal number of output drivers, which may be enabled and disabled (CL2, L66 to CL3, L41; CL5, L9-22; Fig 1), as that allows the mixed analog/digital chip to be divided into analog blocks and digital blocks and using multiplexers connected to the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers (CL1, L52-58). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO, AB** and **PO** with the method of **LE** that included at least one of the flip-flops to be coupled to an equal number of pads through an equal number of output drivers, which may be enabled and disabled, as that would allow the mixed analog/digital chip to be divided into analog blocks and digital blocks and using multiplexers connected to the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers.

10.2 As per Claim 17, **IN, BO, AB, PO** and **LE** teach the method of claim 16. **IN, BO, AB** and **PO** do not expressly teach that the testing of the analog circuit portion is performed while enabling and disabling the output drivers. **LE** teaches that the testing of the analog circuit portion is performed while enabling and disabling the output drivers (CL2, L66 to CL3, L41; CL5, L9-22; Fig 1), as that allows the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers (CL1, L52-58). It would have been obvious to one of ordinary skill in the art at the time of

Applicant's invention to modify the method of **IN, BO, AB** and **PO** with the method of **LE** that included the testing of the analog circuit portion being performed while enabling and disabling the output drivers, as that would allow the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers.

11. Claims 18 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), and further in view of **Perkins et al. (PE)** (U.S. Patent 6,625,557).

11.1 As per Claim 18, **IN** and **BO** teach the method of claim 1. **IN** and **BO** do not expressly teach that the analog circuit portion includes an RF circuit subportion. **PE** teaches that the analog circuit portion includes an RF circuit subportion (CL1, L52-54; CL6, L1-32), as that allows testing analog circuits with radio frequency signals (CL6, L1-32). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** and **BO** with the method of **PE** that included the analog circuit portion including an RF circuit subportion, as that would allow testing analog circuits with radio frequency signals.

11.2 As per Claim 42, **IN** and **BO** teach the integrated circuit of claim 36. **IN** and **BO** do not expressly teach that the analog circuit portion includes an RF circuit subportion. **PE** teaches that the analog circuit portion includes an RF circuit subportion (CL1, L52-54; CL6, L1-32), as that allows testing analog circuits with radio frequency signals (CL6, L1-32). It would have been

obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN** and **BO** with the integrated circuit of **PE** that included the analog circuit portion including an RF circuit subportion, as that would allow testing analog circuits with radio frequency signals.

12. Claims 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), and further in view of **Okazaki et al. (OK)** (U.S. Patent 6,282,503).

12.1 As per Claim 31, **IN** teaches a method of designing an integrated circuit having digital and analog circuit portions, the digital and analog circuit portions each having defined functions (CL1, L26-32); comprising:

providing an emulation circuit which comprises a plurality of logic circuits (CL1, L7-11; CL1, L63-66);

affixing the emulation circuit on the integrated circuit (CL1, L63 to CL2, L4; CL2, L30-39);

providing a version of the analog circuit portion having at least some of the defined functions of the analog circuit portion (CL1, L63 to CL2, L4);

affixing the analog circuit version on the integrated circuit (CL1, L63 to CL2, L4);

testing the analog circuit version (CL2, L4-6; CL1, L36-37; CL2, L30-39); and

providing the digital circuit portion (CL1, L41-43; CL1, L63-66; CL1, L22).

IN does not expressly teach providing an emulation circuit, which is capable of generating noise, and which comprises a plurality of logic elements. **BO** teaches providing an emulation circuit, which is capable of generating noise, and which comprises a plurality of logic elements (Abstract; CL1, L19-30; CL1, L58-63), as generating and applying noise permits evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included providing an emulation circuit, which was capable of generating noise, and which comprised a plurality of logic elements, as generating and applying noise would permit evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit.

IN does not expressly teach that the digital circuit portion may be formed by rewiring the emulation circuit. **OK** teaches that the digital circuit portion may be formed by rewiring the emulation circuit (Abstract; CL1, L33-35; CL1, L43-49), as that allows not only logic verification, but also determining the specification of the target logic circuit (CL1, L65-67); utilizing the logic emulation allows the performance of the target circuit to be measured while its design is being varied until an optimum design is achieved (CL2, L10-14). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **OK** that included the digital circuit portion being formed by rewiring the emulation circuit, as that would allow not only logic verification, but also

determining the specification of the target logic circuit; utilizing the logic emulation would allow the performance of the target circuit to be measured while its design was being varied until an optimum design was achieved.

As per Claim 32, **IN** teaches modifying the analog portion in response to the testing (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

12.2 As per Claim 33, **IN, BO** and **OK** teach the method of claim 31. **IN** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion is obtained (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

IN does not expressly teach repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained. **BO** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained (CL1, L50-54), as that would minimize performance degradation of an analog or mixed signal integrated circuit (CL1, L50-54). It would

have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained, as that would minimize performance degradation of an analog or mixed signal integrated circuit.

As per Claim 34, **IN** teaches reconnecting the logic elements to provide for the digital portion (CL2, L30-39).

12.3 As per Claim 35, **IN, BO** and **OK** teach the method of claim 31. **IN** does not expressly teach that the noise generated by the emulation circuit is substantially equivalent to the digital circuit portion. **BO** teaches that the noise generated by the emulation circuit is substantially equivalent to the digital circuit portion (Abstract, L3-5), as that permits applying the noise for the evaluation of possible degradation of an analog or mixed signal circuit to determine the need for effective noise suppression and design modifications of the circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included the number of gates in the emulation circuit being substantially equivalent to a number of gates in the digital circuit portion, as that would permit noise to be generated representative of the digital switching noise generated by the digital integrated circuit.

Arguments

13.1 As per the applicants' argument that "**Insenser Farre. (IN)** and **Boerstler et al.** do not teach providing the digital circuit portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the emulation circuit", the Examiner respectfully disagrees. **Insenser Farre.** teaches providing the digital circuit portion, the design of which is based on the testing of the analog circuit version (CL1, L35-36; CL2, L30-39; the programmable digital portion allows modifying the design of the digital portion based on the testing of the analog circuit version); while modifying the configuration of the emulation circuit (CL1, L21-22; CL2, L14-19; CL2, L22-26; CL1, L63-66).

13.2 As per the applicants' argument that "**Insenser Farre. (IN)** and **Boerstler et al.** do not teach providing the digital circuit portion, wherein the digital circuit portion may be formed by rewiring the emulation circuit", the Examiner respectfully disagrees. **Insenser Farre.** teaches providing the digital circuit portion (CL1, L41-43; CL1, L63-66; CL1, L22). **Okazaki et al.** teaches that the digital circuit portion may be formed by rewiring the emulation circuit (Abstract; CL1, L33-35; CL1, L43-49)

Conclusion

ACTION IS FINAL – NECESSIATED BY AMENDMENT

14. Applicant's amendments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
July 16, 2004